



PIC16F73/74/76/77

PIC16F73/74/76/77 Rev. B1 Silicon/Data Sheet Errata

The PIC16F73/74/76/77 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS30325B), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16F73/74/76/77 silicon.

1. Module: Timer1

When Timer1 is running in Asynchronous mode and then disabled, data in the Timer1 register (TMR1) may become corrupted. Corruption occurs when the timer enable is turned off at the same instant that a ripple carry occurs in the timer module.

This issue only occurs in asynchronous operation. In synchronous operation, the relevant signals are latched with the CPU clock and the problem condition does not arise.

Revision C silicon will correct this issue.

Work around

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become corrupted.

If an application requires that Timer1 be turned off, and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first by clearing the T1SYNC bit of register T1CON (T1CON<2>). Please note, however, that this may cause Timer1 to miss up to one count.

Date Codes Pertaining To This Issue

PIC16F73/74	0219 and earlier
PIC16F76/77	0303 and earlier

2. Module: CCP (Compare Mode)

The output of the CCP module in Compare mode may become inverted when the mode of the module is changed from Compare/Clear on Match (CCPxM<3:0> = 1001) to Compare/Set on Match (CCPxM<3:0> = 1000). This may occur as a result of any operation that selectively clears bit CCPxM0, such as a BCF instruction.

When this condition occurs, the output becomes inverted when the instruction is executed. It will remain inverted for all following Compare operations, until the module is reset.

Revision C silicon will correct this issue.

Work around

Do not selectively clear bit CCPxM0 to select the Compare/Set on Match mode. Instead, clear the entire CCPxCON register, which resets the module. Follow this with an instruction to set CCPxM3 (CCPxCON<3>), which selects the Set on Match mode.

Date Codes Pertaining To This Issue

PIC16F73/74	0219 and earlier
PIC16F76/77	0303 and earlier

PIC16F73/74/76/77

3. Module: Oscillator (HS mode)

When resonators above 2 MHz are used, the HS mode oscillator is required to ensure reliable operation. HS mode oscillator drive at frequencies from 2 MHz to 4 MHz is often excessive, resulting in the amplitude of the oscillator waveform exceeding V_{DD} and V_{SS} . In such cases, the waveform may experience distortion as ESD protection devices begin to operate on the OSC1 and OSC2 pins. This distortion appears as a non-sinusoidal waveform or clipping, and can generate substantial harmonics that may create excessive noise in the application.

Revision C silicon will correct this issue.

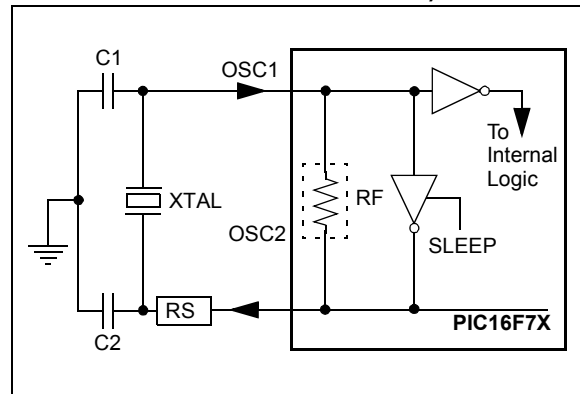
Work around

The gain of the oscillator should be reduced by inserting a series resistance between the OSC2 pin and the resonator/capacitor as shown in the data sheet (see Figure 1). The value of the series resistance is dependant on V_{DD} , resonator frequency, and temperature; however, 330 ohms has been used as a good starting point for evaluation.

This change will not affect operation of future revisions of silicon as long as HS mode is selected.

Note: This issue applies only to resonators above 2 MHz in Revision B silicon. No issues are known to exist with crystals at any frequency using XT Osc mode.

FIGURE 1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Date Codes Pertaining To This Issue

PIC16F73/74	0219 and earlier
PIC16F76/77	0303 and earlier

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30325B), the following clarifications and corrections should be noted.

1. Module: Core

The typical and maximum supply currents (parameter D010A) specified for extended voltage devices have been changed.

The IDD specifications differ from the Device Data Sheet only for devices operating at a VDD of 3.0V and a Fosc of 32 kHz, with the WDT disabled.

The changes in the specification are shown in **bold** in Table 1.

Work around

None.

Date Codes Pertaining To This Issue

All.

TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic/ Device	New Specification			Data Sheet Specification			Units	Notes
			Min	Typ	Max	Min	Typ	Max		
D010A	IDD	Supply Current PIC16LF73/74/76/77	—	25	48	—	20	48	μA	LP osc configuration, Fosc = 32 kHz, VDD = 3.0V, WDT disabled

PIC16F73/74/76/77

2. Module: Pinout Correction

The MLF (now known as QFN) package pinout locations for pins RA4 and RA5 were incorrectly stated in Table 2-1 of the Device Data Sheet.

The correct pinout locations are indicated in **bold** in Table 2.

TABLE 2: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
RA4/T0CKI RA4 T0CKI	6	3	I/O I	ST	Digital I/O – Open drain when configured as output. Timer0 external clock input.
RA5/ <u>SS</u> /AN4 RA5 <u>SS</u> AN4	7	4	I/O I I	TTL	Digital I/O. SPI slave select input. Analog input 4.

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
 3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

REVISION HISTORY

Rev A Document (2/01)

Original errata document for PIC16F77 (DS80099A). Issue 1 (Timer1), page 1.

Rev B Document (4/01)

Addition of other members of 16F7X family for Issue 1.

Added Issue 2 (Core), page 1, and Issue 3 (A/D), page 2.

Rev C Document (7/01)

Added Issue 4 (CCP), page 2, and Issue 5 (Core), page 3.

Rev D Document (8/01)

Under Clarifications/Corrections to the Data Sheet, added Issue 1 (Reset), page 4.

Rev E Document (9/02)

Removed previous Clarifications/Corrections to the Data Sheet (DS30325A), added Issue 6 (Oscillator), page 4.

Rev F Document (1/03)

Removed previous silicon issue 2 (Core) and silicon issue 3 (A/D), and updated silicon issue 1 (Timer1), silicon issue 2, (formerly issue 4, Compare Mode), and silicon issue 3 (formerly issue 6, HS Mode) with new date code information. Moved previous silicon issue 5 (Core) to Clarifications/Corrections to the Data Sheet (DS30325B) and added issue 2 (Pinout Correction).

PIC16F73/74/76/77

NOTES:

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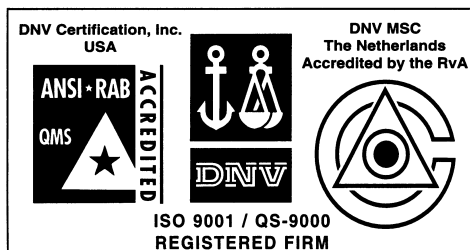
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